



IEEE 802.16e (WiMAX) and IEEE 802.11n (WiFi) LDPC Decoder IP core

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Overview

Error-correcting coding is an essential tool for enabling reliable communication. Unicore Systems provide an Intellectual Property (IP) core for hardware-efficient implementation of low-density parity-check (LDPC) forward error correcting (FEC) schemes intended for the IEEE 802.16e [1] and for the 802.11n[2]. The IP core covers the entire WiMaX and WiFi LDPC specification, in terms of block size and code rate. WiFi mode, WiMax mode, block size and code rate can be switched on a block-by-block basis.

Key Features

- WiMax 19 code length supported (Z factor 24,28...96);
- WiFi 3 code length supported (Z factor 27,54,81);
- WiMax all code rates 1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6 supported;
- WiFi all code rates 1/2, 2/3, 3/4, 5/6 supported;
- parameterized input data width 5-8 bit (in compilation phase);
- parameterized internal data width 6-9 bit (in compilation phase);
- nearly floating point performance with quantization of 5 input bits and internal computation in 8 bits (less than 0.15 dB from floating point BP with 30 iterations);
- early stop detection unit ;
- parallelism degree 96;
- bit-LLR input
- decoded throughput up to 193 Mbit/sec (Virtex-4 -12 speed grade) for WiMax mode. (Z=96, 15 iterations, Fclk=160 MHz)
- decoded throughput up to 164 Mbit/sec (Virtex-4 -12 speed grade) for WiFi mode. (Z=81, 15 iterations, Fclk=160 MHz)
- Free LDPC Encoder IP core comes with the Decoder

Applications

- IEEE 802.16e (WiMax) systems
- IEEE 802.11n (WiFi) systems
- Wireless communications
- Backhaul Base Station
- High Speed Link

Functional Description

The decoder design is fully synchronous on a single input system clock. LDPC decoder uses layered offset min-sum belief propagation technique which converges twice as fast as the standard belief propagation algorithm, resulting in twice the throughput and was designed using sequentially-concurrent architecture. In order to detect that the correct codeword is found, two sets of tests are performed in early stop detection unit after finishing the decoding of each layer. IP core contains input and output buffer to ease integration into user system. The Data Input Interface accepts a set of channel observation data in the form of quantized Log-Likelihood on coded bits (bit-LLRs). The Data Output Interface yields the results in the form of hard decision bits. The decoder IP core allows each frame to be monitored and controlled via dedicated configuration pins. Activating the early stop detection function allows reducing power consumption, as the average number of iterations performed decreases especially at low decoded BER operating points. It also decreases the average latency. It might be used to increase the average throughput of the decoder, provided that the system instantiating the decoder is able to deal with variable decoding delays.

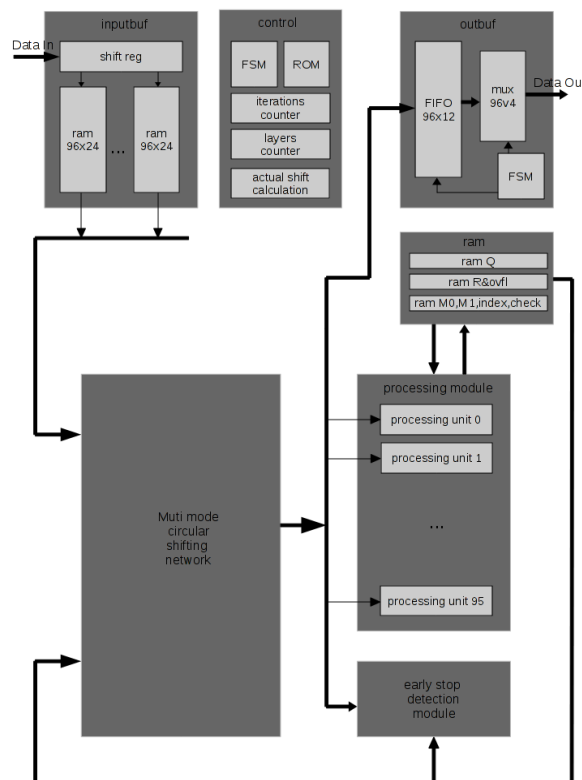
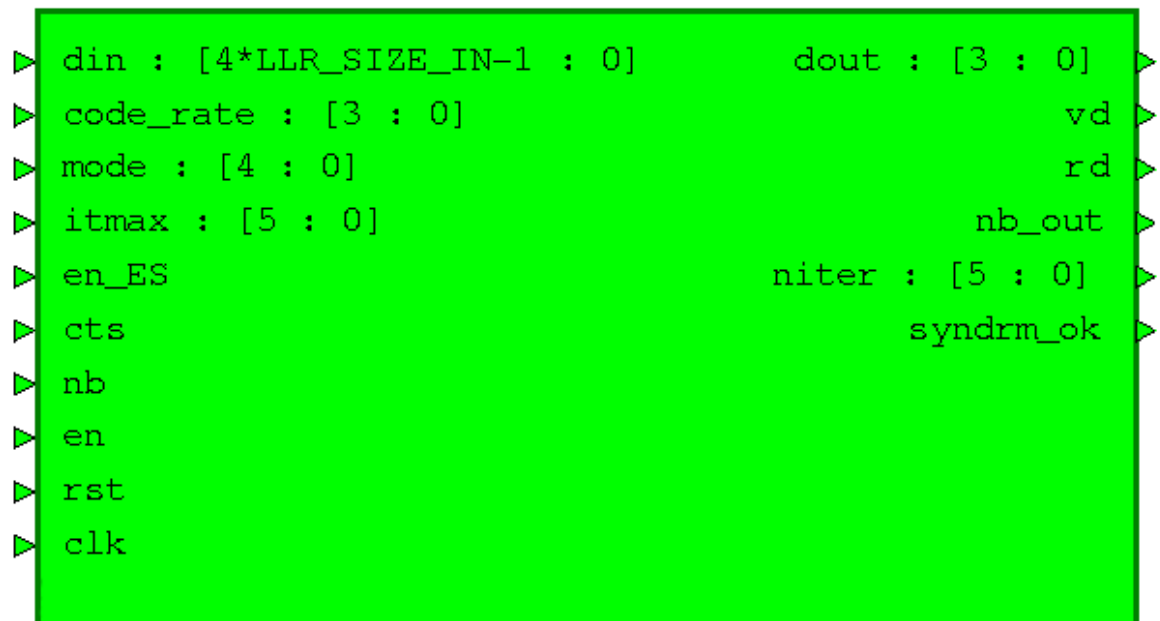


Figure 1. Block diagram of the decoder.

Core I/O signals

The LDPC decoder core symbol is illustrated in Figure 2.

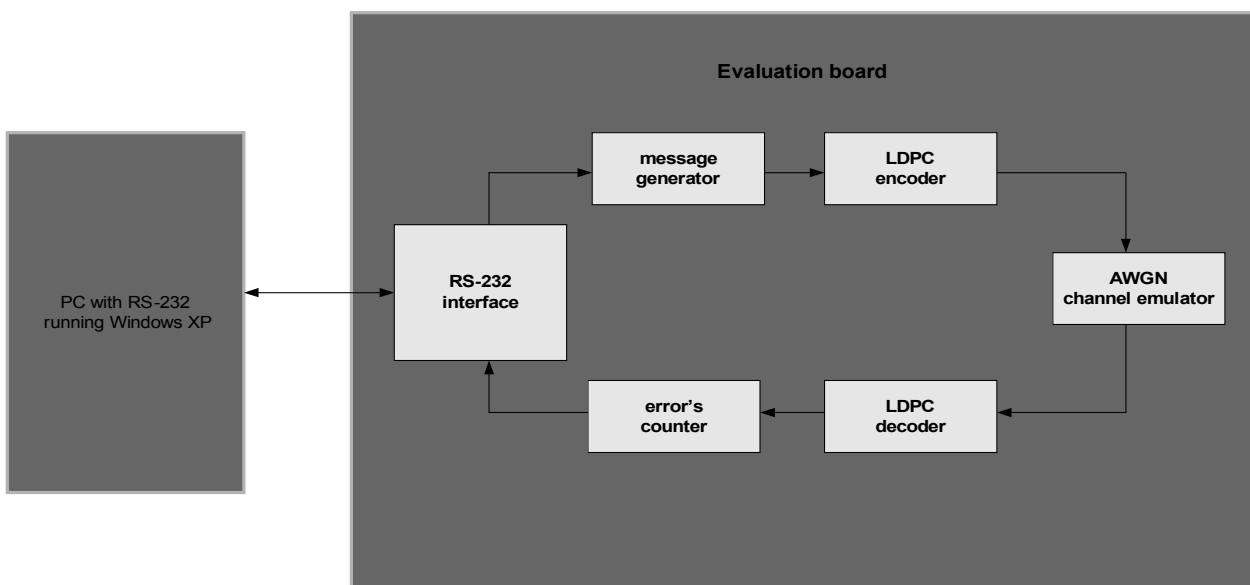


Signal	Type	Description
clk	input	Clock signal input (rising edge)
rst	input	Synchronous reset of encoder IP core.
en	input	Enable: set high when data is valid on din .
nb	input	New block strobe. Indicates a new block.
cts	input	Clear to send from host
en_es	input	Enable early stop detection unit
itmax[5:0]	input	Maximum number of iterations
mode[4:0]	input	Code block size parameters (Z): 00000 - 00101 RESERVED <i>WiMax</i> 00110 -Z=24

		0011 –Z=28 1011 –Z=92 11000 –Z=96 <i>WiFi</i> 11001 –Z=27 11010 –Z=54 11011 –Z=81 11001 - 11111 RESERVED
code_rate[3:0]	input	Code rate parameters: <i>WiMax</i> 0000 –R=5/6 0001 –R=3/4B 0010 –R=3/4A 0011 –R=2/3B 0100 –R=2/3A 0101 –R=1/2 <i>WiFi</i> 1000 –R=5/6 1001 –R=3/4 1010 –R=2/3 1011 –R=1/2 1000 - 00101 RESERVED others –RESERVED
din[4*LLR_SIZE_IN-1:0]	input	Input information
dout[3:0]	output	Hard decisions from decoder. Bit 3 is first bit of information in half byte.
vd	output	Valid data. vd is asserted by the core to indicate that data on dout is valid.
rd	output	Ready –is asserted by the core to indicate that it is ready for loading data into input buffer.
nb_out	output	New block on output.
niter[5:0]	output	Number of iterations made by decoder.
syndrm_ok	output	Signal indicates that output code word is valid .

Hardware Verification

The LDPC decoder IP core has been hardware verified on DE2-70 board with Altera Cyclone-II and ADS-XLX-V4LX-EVL60 board with Xilinx Virtex-4. And also it has been thoroughly tested in a testbench suite. A software reference design is available upon request. The platform also includes a GUI type interface to allow the user to experiment with the parameters of the LDPC decoder. The platform is useful for exploring the configuration settings of the LDPC decoder and for obtaining low BER results. Block diagram of the hardware evaluation system is depicted in the Figure 3.



Simulation software

Simulation software (runs under Windows OS and Linux OS) delivered with this IP core implements exact fixed point model of LDPC decoder and can be used for performance simulation and test vector generation for verification. Within simulator user can vary miscellaneous parameters of IP core (input data width, internal data width, offset min-sum parameters, maximum number of iterations) and predict the performance of hardware realization. Software generates text files with AWGN added to coded data and expected decoder output for efficient verification. The IP core is provided with a range of script files and a testbench to functionally simulating LDPC decoder design.



Design Features

- Technology Independent
- Fully Synchronous Design with no Latches
- Highly Modular Design with clearly defined interfaces
- Scan friendly RTL
- Consistent coding procedures

Implementation details

These implementation results are given for 5 bits input quantization and internal data width set to 8 bit

Xilinx ISE 11 report for XC4VLX60-12:

Number of occupied Slices:	22,212	out of	26,624	83%
Number of FIFO16/RAMB16s:	27	out of	160	16%
Number of DSP48s:	1	out of	64	1%

Deliverables

- RTL Verilog source code or synthesized netlist;
- Full Verilog Test environment (Selfchecking);
- Fixed point software model running under Windows for simulation and test patterns generation;
- User guide, test specification and scripts.
- Reference design
- Example Synthesis scripts
- 3 months free email support to ensure successful integration into the customer's system
- Changes to the internal design to meet customer requirements are possible

Ordering Information

This product is available directly from Unicore Systems Ltd under the IP License. To purchase or make further inquiries about this IP core or any other Unicore Systems products and services please contact us at the address specified on the front page.

References

- [1] "Part 16: Air Interface for Fixed and Mobile Broadband Wireless Access Systems Amendment for Physical and Medium Access Control Layers for Combined Fixed and Mobile Operation in Licensed Bands", IEEE P802.16e-2005, October 2005.
- [2] IEEE 802.11n. Wireless LAN Medium Access Control and Physical Layer specifications: Enhancements for Higher Throughput. IEEE P802.16n/D1.0, Mar 2006.

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