

### *IEEE 802.16e (WiMAX) LDPC Encoder IP core*

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#### **Overview**

Error-correcting coding is an essential tool for enabling reliable communication. Unicore Systems provide an Intellectual Property (IP) core for efficient implementation of low-density parity-check (LDPC) forward error correcting (FEC) encoding schemes intended for the IEEE 802.16e [1]. The IP core covers the entire WiMAX LDPC specification, in terms of block size and code rate. Block size and code rate can be switched on on a block-by-block basis.

#### **Key Features**

- 19 code length supported;
- all ratio 1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6 supported;
- on the fly change of code length and code ratio;
- encoded throughput up to 600 Mbit/sec (Virtex-4 -12 speed grade).
- Low latency

#### **Functional Description**

The decoder design is fully synchronous on a single input system clock. IP core contains input and output buffer to ease integration into user system.

#### **Applications**

- IEEE 802.16e (WiMax) systems
- Wireless communications
- Backhaul Base Station
- High Speed Link

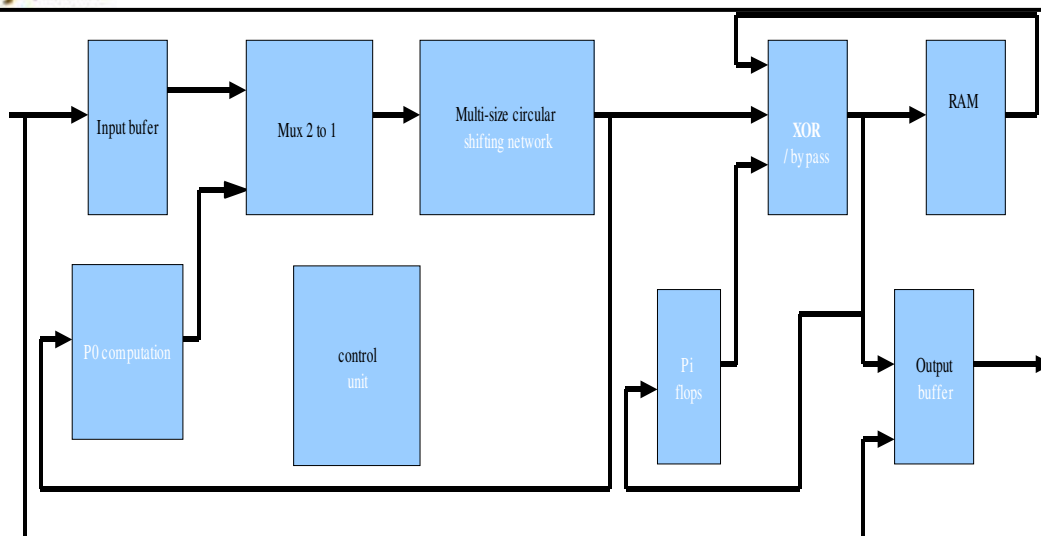


Figure 1. Block diagram of the encoder.

## Core I/O signals

The LDPC encoder core symbol is illustrated in Figure 2.

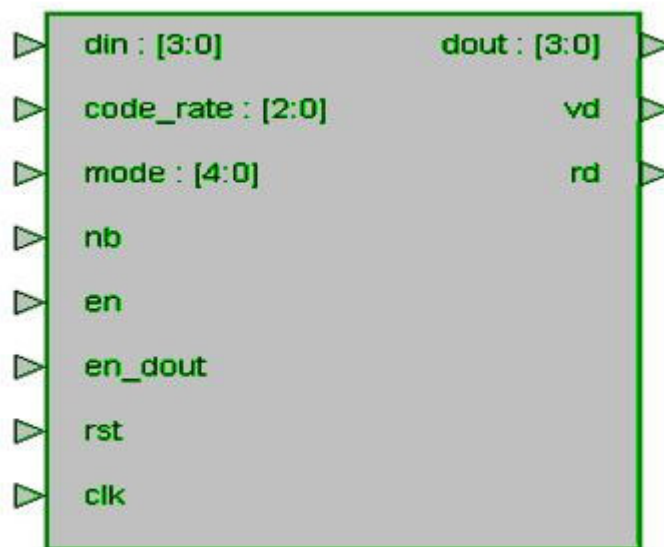


Figure 2. LDPC encoder IP core symbol

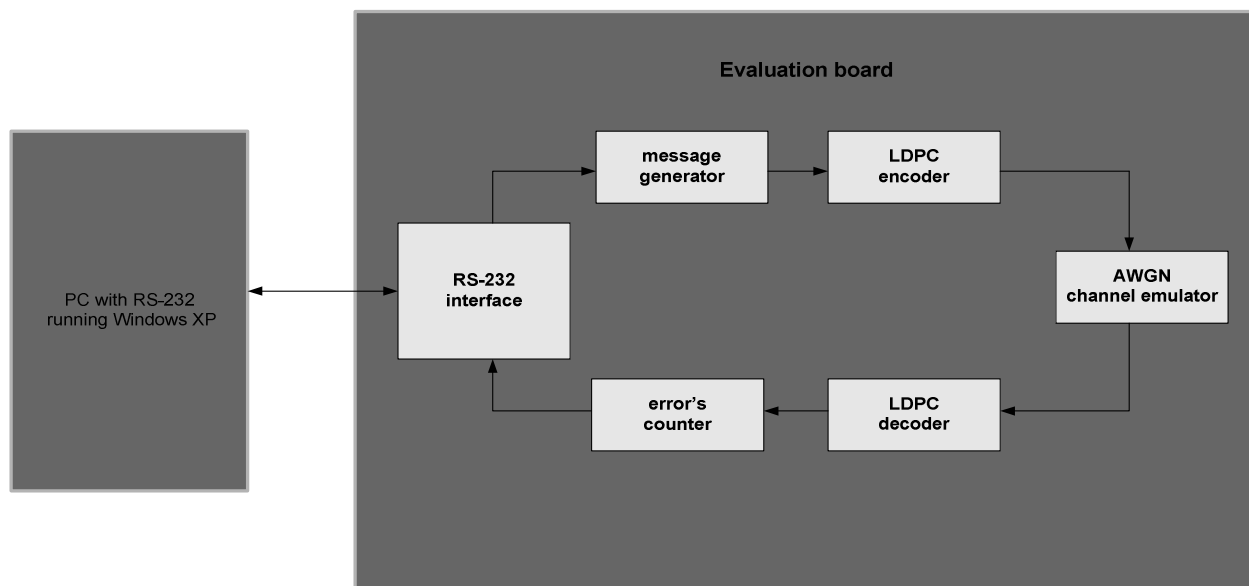
Signal	Type	Description
<b>rst</b>	input	Synchronous reset of encoder IP core.
<b>clk</b>	input	Clock signal input (rising edge)
<b>nb</b>	input	New block strobe. Indicates a new block. Falling edge of new block forces decoder to start decoding loaded data. Decoding should be started only when

		<b>rd</b> signal is high. <b>nb</b> must be held high while information is loading
<b>code_rate[2:0]</b>	input	Code rate parameters: <b>000 -R=5/6</b> <b>001 -R=3/4B</b> <b>010 -R=3/4A</b> <b>011 -R=2/3B</b> <b>100 -R=2/3A</b> <b>101 -R=1/2</b> <b>110,111 -RESERVED</b>
<b>mode[4:0]</b>	input	Code block size parameters (Z): <b>00000 - 00101 RESERVED</b> <b>00110 -Z=24</b> <b>00111 -Z=28</b> ..... ..... <b>10111 -Z=92</b> <b>11000 -Z=96</b> <b>11001 - 11111 RESERVED</b>
<b>en</b>	input	Enable: set high when data is valid on <b>din</b> .
<b>din[4*`WORD_SIZE_IN-1:0]</b>	input	Input information
<b>en_es</b>	input	Enable early stop detection unit
<b>rd</b>	output	Ready –is asserted by the core to indicate that it is ready start decoding of data loaded into input buffer. Decoding process is started by last clock under active <b>nb</b> signal.
<b>vd</b>	output	Valid data. VD is asserted by the core to indicate that data on <b>dout</b> is valid.
<b>dout[3:0]</b>	output	Hard decisions from decoder. Bit 3 is first bit of information in half byte.

**Note:** **Code\_rate** and **mode** settings must be valid all time whilst **nb** signal is high.

### Verification description

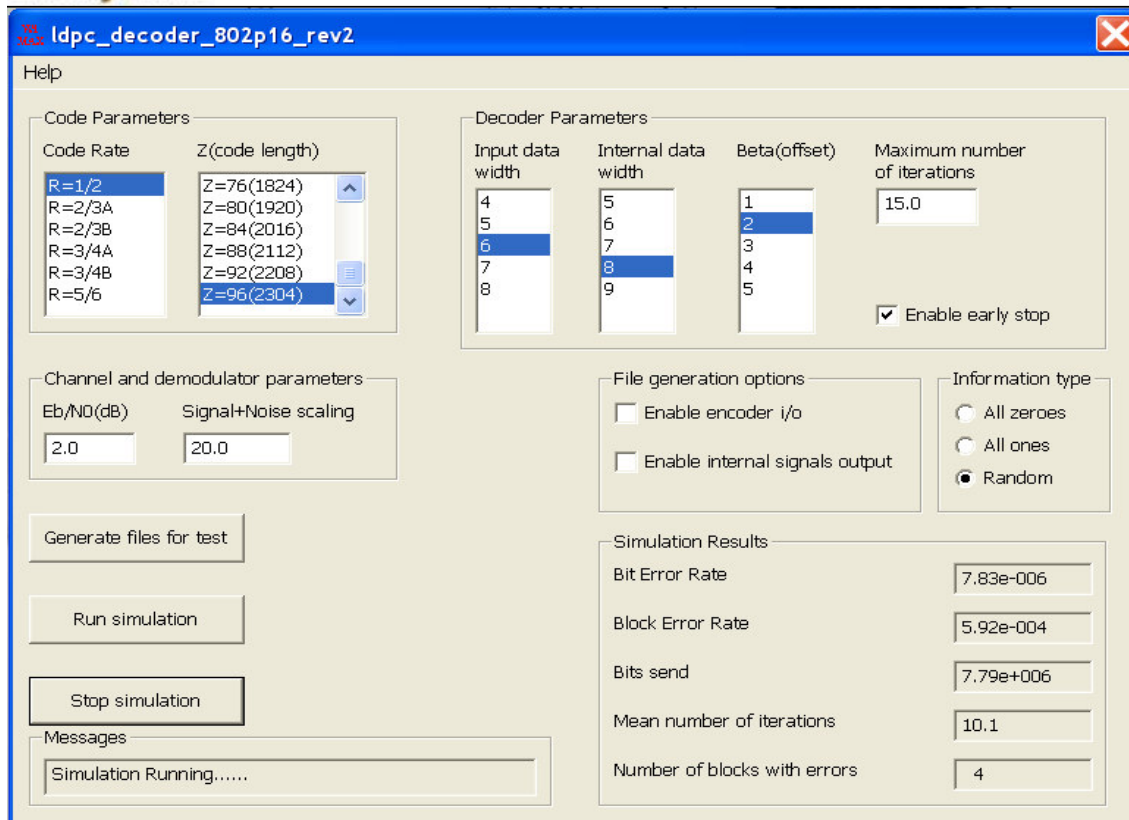
The LDPC decoder IP core has been hardware verified on DE2-70 board with Altera Cyclone-II and ADS-XLX-V4LX-EVL60 board with Xilinx Virtex-4. And also it has been thoroughly tested in a testbench suite. A reference design is available upon request. The platform also includes a GUI type interface to allow the user to experiment with the parameters of the LDPC decoder. The platform is useful for exploring the configuration settings of the LDPC encoder and for obtaining low BER results. Block diagram of the hardware evaluation system is depicted in the Figure 3.



**Figure 3. Block diagram of hardware evaluation platform.**

### Simulation software

Simulation software (runs under Windows OS) delivered with this IP core implements exact fixed point model of LDPC decoder and can be used for performance simulation and test vector generation for verification. Within simulator user can vary miscellaneous parameters of IP core (input data width, internal data width, offset min-sum parameters, maximum number of iterations) and predict the performance of hardware realization. Software generates text files with AWGN added to coded data and expected decoder output for efficient verification.



**Figure 4. Simulation software.**

## Design Features

- Technology Independent
- Fully Synchronous Design with no Latches
- Highly Modular Design with clearly defined interfaces
- Scan friendly RTL
- Consistent coding procedures

## Implementation details

Xilinx ISE 10.1 report for 4vlx15ff676-12:

Number of occupied Slices:	2,554	out of	6,144	41%
Number of FIFO16/RAMB16s:	1	out of	48	2%
Number of DSP48s:	1	out of	32	3%

Quartus 8.1 report for EP2S15F484C3:

Combinational ALUTs :	2,430
Total registers :	1,165
Total block memory bits :	11,960
DSP block 9-bit elements :	2

These synthesis results are provided for reference only. Please contact us for estimates for your application

### **Deliverables**

- RTL Verilog source code or synthesized netlist;
- Full Verilog Test environment (Selfchecking);
- Fixed point software model running under Windows for simulation and test patterns generation;
- User guide, test specification and scripts.
- Reference design
- Example Synthesis scripts
- 3 months free email support to ensure successful integration into the customer's system
- Changes to the internal design to meet customer requirements are possible

### **Ordering Information**

This product is available directly from Unicore Systems Ltd under the IP License. To purchase or make further inquiries about this IP core or any other Unicore Systems products and services please contact us at the address specified on the front page.

### **References**

[1] "Part 16: Air Interface for Fixed and Mobile Broadband Wireless Access Systems Amendment for Physical and Medium Access Control Layers for Combined Fixed and Mobile Operation in Licensed Bands", IEEE P802.16e-2005, October 2005.